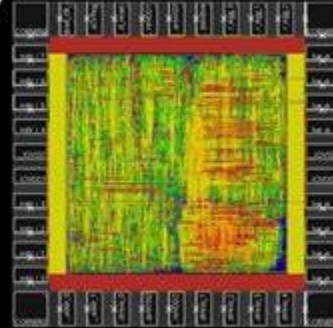


RISC-V

Libre Computing



Freedom hardware: Current state and forward looking statements

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The RISC-V architecture and ecosystem have undergone tremendous growth recently. We will take a look at the current state of RISC-V and its current deployment footprint. We'll discuss where RISC-V may be headed and the role it may play in completely open and free datacenter servers, tablets, and cellphones. We will review the emergence of the ARM architecture and how it may be an important stepping stone to a free computing platform. We'll discuss the differences between the ARM licensing model and the X86_64 architecture licensing model as well as the role of ARM processors in cell phones and cloud datacenters (such as AWS). Finally, we'll take a brief look at some options for starting RISC-V free and open hardware development for both experienced FPGA programmers and newbies. We'll explain options including physical RISC-V processors, FPGAs, and software emulation.

What is RISC-V

- Instruction Set Architecture (ISA)
- ISAs Are Licensed Like Software
- Other Active ISAs:
 - x86_64 (Intel, AMD)
 - ARM64 (CPU: Graviton; SoC: A16, Snapdragon)
- Licensing Status
 - RISC-V (Open, Libre, Extensible, Free [BSD])
 - x86_64 (Proprietary, Not Extensible, Very Expensive)
 - ARM64 (Extensible, Somewhat Expensive)

Current State of ISAs

x86_64: Mature, High Performance, Very Broad Support

- Examples: Intel/AMD Datacenter Servers, Desktops,
Laptops

ARM64: Less Mature, Good Performance, Broad Support

- Examples: AWS Graviton, Apple, Cellphones, Tablets

RISC-V: Developing, OK Performance, OK Support

- Examples: Dev Boards (primarily), SoC Devices,
Embedded Devices, Task Offloading (Daughter
Processors/Boards [Nvidia GPUs])

X86_64 => ARM64 => RISC-V? GNU Parallel?

- Historically ISAs were proprietary intellectual property (think Oracle)
- x86_64 brought collaboration (Intel & AMD); small step toward openness
- ARM64 brought lower cost and more broad licensing policy - larger step toward openness
- What Did ARM Licenses Look Like?
 - ARM licenses based on usage of CPUs
 - Some companies got perpetual licenses (Apple, Amazon?)
 - ARM would license to pretty much anyone
 - Often 10% or more of die free for special use (Example: Amazon's "Everything is the network", TLS, Sockets)
 - Possible to add instructions to ARM, but not easy ARM Corp decides

What About RISC-V

- Libre (BSD, mostly), take it if you want it
- Compatibility? That's handled with flags
- Instructions and flags can be added through an Open Standards process
 - Examples:
 - RVV (Vector Extensions (like Intel SSE & SSE2))
 - Crypto (US/NIST - AES/SHA, Russian - Ghost)
- Progression:
 - Microsoft (Booooo!) => GNU/Linux => GNU
 - Intel/AMD/SGI/IBM/etc => ARM64 => RISC-V

Amazon, Apple, Cloud Providers

- Will Amazon Move to RISC-V?
 - Perpetual License (ARM is Cost Free, RISC-V is Cost Free)
 - Which Develops Faster?
 - Libre Software Native Developed on RISC-V?
 - Extension Porting (TCP/IP, Crypto, TLS)
 - Validation and Testing Workloads
 - ARM64 Everywhere in AWS
 - I Run Almost All My MIT Workloads on ARM64 (Graviton)
 - AWS Lambda (ARM64, Whether You Want It Or Not)
 - Similar Story With Apple and Google (Tau 2A)
 - Other Cloud Providers (Hetzger, Rackspace... Yandex)
 - Very Different Story
 - Especially Yandex

Politics: Sanctions

- Russia & China Need Chips
 - Not Just Weapons: Medical Devices; Cars; Traffic Lights; HVAC; TVs; Phones; Washing Machines; Everything!
- ARM Canceled All Russian Licenses
- How Fast Will RISC-V Develop if Russia & China Make An Emergency Move To It?
- Note: Russia Has Proprietary VLIW ISA Elbrus Developed by MCST
- Elbrus Tested vs Intel by Yandex - Test Failed
- Security: Can You Trust Proprietary Chips?
 - Pentium90 FPDIV Bug (Design)
 - Crypto Bugs (SHA3 Overflow) (Software/Standard)
 - Backdoors? (Hardcoded Credentials) (Design)
 - Stealthily Doped Gates (Manufacturing)

Getting Started With RISC-V

- Ubuntu has RISC-V images; Debian (same)
- C/C++; Python; Golang; Rust; Ruby; Java; etc...
- QEMU Emulation (How GNU/Linux packages are built)
 - Built in RISC-V 32bit and RISC-V 64bit cores
- FPGA (Download Verilog RISC-V off Github)
- RISC-V hardware (DevBoards: MangoPi, SciFive, StarFive (Chinese))

Forward Looking Statements

- “Software is eating the world.” - Marc Andreessen
- Libre software/hardware evolves faster and has more eyes (less bugs/security issues)
- Libre software/hardware is cheaper
- A Libre CPU is inevitable and RISC-V the most likely candidate there for RISC-V is inevitable
- AI can help with hardware design
 - Altium Designer (7-Layer board path timing, EM interference prevention trace and component spacing)
 - Google chip design lead MIT AI Lab talk
 - Google uses AI to help design chips at the gate level
- Imagine the future full stack is all Libre software (including CPU)
 - Imagine a profiler can make RISC-V CPU design adjustments/decisions
 - Lots of AES128 crypto? More AES128 crypto modules
 - Lots of network traffic? More L2 cache and paths to RAM/NIC
 - Simulations w/ bignum math? More 1024bit vector registers

Leading Alternative FOSSi Hardware Options

- 1) RISC-V . <https://riscv.org/>
- 2) MIPS (Early Playstation consoles)
- 3) OpenRISC, DLX, and predecessors
- 4) J-Core, formerly SuperH from Hitachi <https://j-core.org/> .
- 5) OpenPiton. <http://www.openpiton.org/>
- 6) Epiphany <https://www.adapteva.com/>
- 7) Nyami
<https://www.cs.binghamton.edu/~millerti/nyami-ispass2015.pdf>
- 8) GPLGPU <https://github.com/asicguy/gplgpu>
- 9) Proof of Life needed. OpenPOWER, OpenSPARC, Geode
- 10) EOLed hardware - with deprecated GNU/Linux port projects

The RV Trade Space

C class microcontroller

32-bit 3-8 stage in-order variant aimed at 50-250 Mhz microcontroller variants

- Optional memory protection Very low power static design
- Fault Tolerant variants for ISO26262 applications
- IoT variants will have compressed/reduced ISA support

I class processors

- 64-bit, 1-4 core, 5-8 stage out of order, aimed at 200-1Ghz industrial control / general purpose applications
- Devices aimed at networking applications will have dual-quad issue support
- Other features – shared L2 cache, AXI bus, threading support

M Class processors

- Enhanced variants of the I-class processors aimed at general purpose compute, low end server and mobile applications
- Enhancements over I class – large issue size, quad-threaded, up to 8 cores, freq up to 2.5 Ghz, optional NoC fabric

S class processors

- 64-bit superscalar, multi-threaded variant for desktop/server applications. 1.2-3Ghz, 2-16 cores, crossbar/ring interconnect, segmented L3 cache
- RapidIO based external cache coherent interconnect for multi-socket applications (up to 256 sockets)
- Hybrid Memory Cube support, 256/512 bit SIMD
- Specialized variants with FUs for database acceleration, security acceleration.
- Experimental variants will be used as test-bed for our Adaptive System Fabric project which aims to design a data-center architecture using NV RAM devices and unified interconnects for memory, storage and networking and leverages persistent memory techniques

H class processors

- 64-bit in-order, multi-threaded, HPC variant with 32-100 cores, 512 bit SIMD, Interconnect TBD
- Goal is 3-5 + Tflops (DP, sustained)

T class processors

Experimental security oriented 64-bit variants with tagged ISA, single address space support, decoupling of protection from memory management.

Leading RV Companies

- 1) SiFive
- 2) RIOS Labs
- 3) Imperas
- 4) Andes
- 5) Esperanto
- 6) Ventana
- 7) Cudasip
- 8) Imagination Technologies
- 9) Renesas, Espressif, Syntacore
- 10) Google, NVidia, Intel, Qualcomm, Seagate

Leading Projects

- 1) Mentorship program <https://riscv.org/risc-v-mentorship-program/>
- 2) RV Exchange <https://riscv.org/exchange/>
- 3) OpenHW. <https://www.openhwgroup.org>
- 4) Chipyard. <https://github.com/ucb-bar/chipyard>
- 5) OpenCompute. <https://www.opencompute.org/>
- 6) <https://lowrisc.org/>
- 7) <https://opentitan.org/>
- 8) <https://opencores.org/>
- 9) <https://www.fossi-foundation.org/>
- 10) Projects List <https://github.com/riscvarchive/riscv-cores-list>

Interesting Products

- 1) MangoPi board
- 2) RV Soldering Iron
- 3) Multiarchitecture.
<https://www.bunniestudios.com/blog/?p=6606>
- 4) Many products on
<https://www.crowdsupply.com/search?q=risc-v>

The Bad News

- 1) Little market penetration in any vertical
- 2) No product in many verticals yet
- 3) HPCwire articles
<https://www.hpcwire.com/2022/11/18/risc-v-is-far-from-being-an-alternative-to-x86-and-arm-in-hpc/>
- 4) Nvidia article [hpcwire.com/2022/09/23/nvidia-shuts-out-risc-v-software-support-for-gpus](https://www.hpcwire.com/2022/09/23/nvidia-shuts-out-risc-v-software-support-for-gpus)

Conferences

- 1) Boston Area Architecture Conference. <https://bostonarch.github.io/2022/>
- 2) RISC-V Summit . <https://riscv.org/event/risc-v-summit-2022/>
- 3) Princeton Comp Arch Day. <https://bit.ly/pton-comp-arch-day-2023>
- 4) LatchUp. <http://latchup.io/>
- 5) Week Of Open Source Hardware <https://www.fossi-foundation.org/wosh/>
- 6) RISC-V lecture next week <https://www.csail.mit.edu/event/risc-v-inevitable>
- 7) Open Hardware Summit <https://2023.oshwa.org/>
- 8) HPC on RV Workshop
<https://riscv.epcc.ed.ac.uk/community/isc23-workshop/>
- 9) MEWD. <https://stamcenter.asu.edu/mewd-workshop/>
- 10) OGHPC (OG = Oil & Gas) <https://www.energyhpc.rice.edu/>
- 11) HPC on Wall Street <https://www.hpcaiwallstreet.com/>

Decidedly Not FOSSi hardware (but interesting in the HPC space)

- 1) Morello Board (CHERI architecture)
- 2) Neocortex WSE
- 3) Lucata, formerly Emu
- 4) Alpha (big in China)
- 5) Y2K snapshot. Sun, SGI, Cray, DEC, Sicortex, Compaq, HPE
- 6) From Debian-ports list : S390, BlueGene, CBE, hppa, ia64
- 7) Further Back Wang, Symbolics, MAI Basic, Kendall Square Research, Thinking Machines, Apollo, Prime, Mercury, Data General, ADI
- 8) Various FPGA based dev boards or SOCs.

RISC-V in the Datacenter

- 1) What workloads can be moved over?
- 2) What unique aspects of the RV design can be taken advantage of?
- 3) Compare to the incumbents (TOP500.org, Green500.org)
- 4) <https://www.opennovation.org/>
- 5) Advancing HPC with RISC-V
<https://youtube.com/watch?v=iFlcJFcOJKk>
- 6) <https://riscv.org/news/2018/10/top-500-article-europeans-budget-1-4-billion-euros-to-build-next-generation-supercomputers/>
- 7) <https://semiengineering.com/is-risc-v-ready-for-supercomputing/>
- 8) https://www.theregister.com/2023/02/08/riscv_hpc/
- 9) <https://semiengineering.com/risc-v-targets-data-center/>


Future Directions

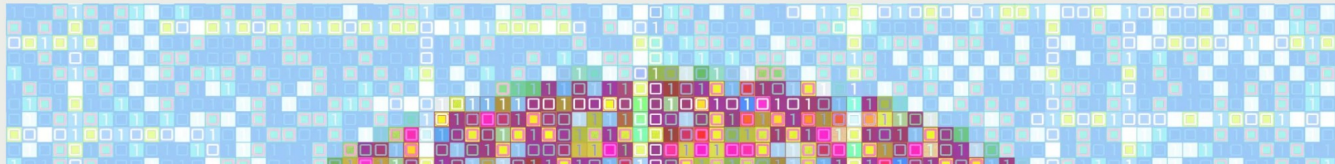
- 1) RV128 <http://rv128.mit.edu/>
- 2) HW / SW Co-design <http://riscv.mit.edu/>
- 3) Posits replacing IEEE 754 Floating Point standard
<https://posithub.org/docs/RISC-V/RISC-V.htm>

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Posits, a New Kind of Number, Improves the Math of AI

> The first posit-based processor core gave a ten-thousandfold accuracy boost

BY DINA GENKINA | 25 SEP 2022 | 4 MIN READ | 



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